

FIG. 1a
(PRIOR ART)

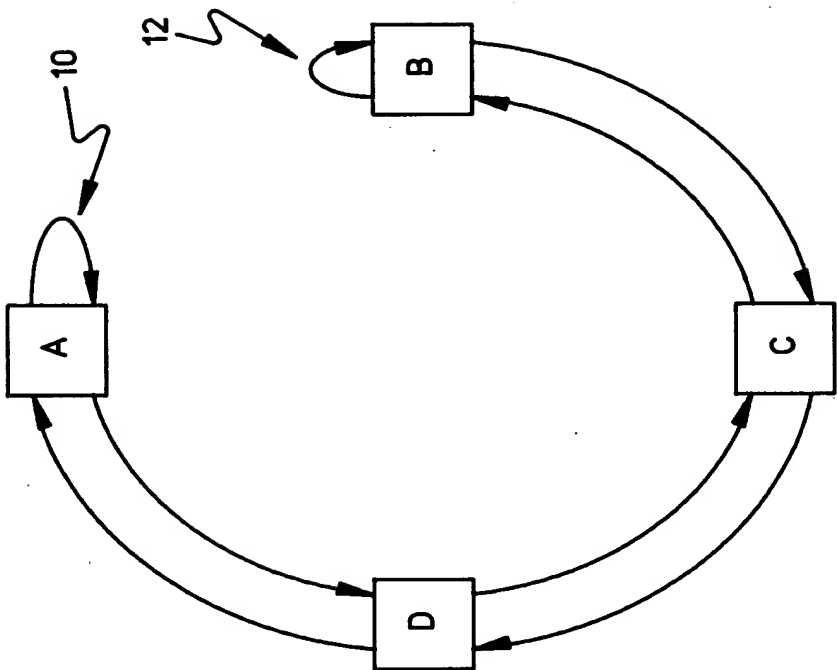


FIG. 1b
(PRIOR ART)

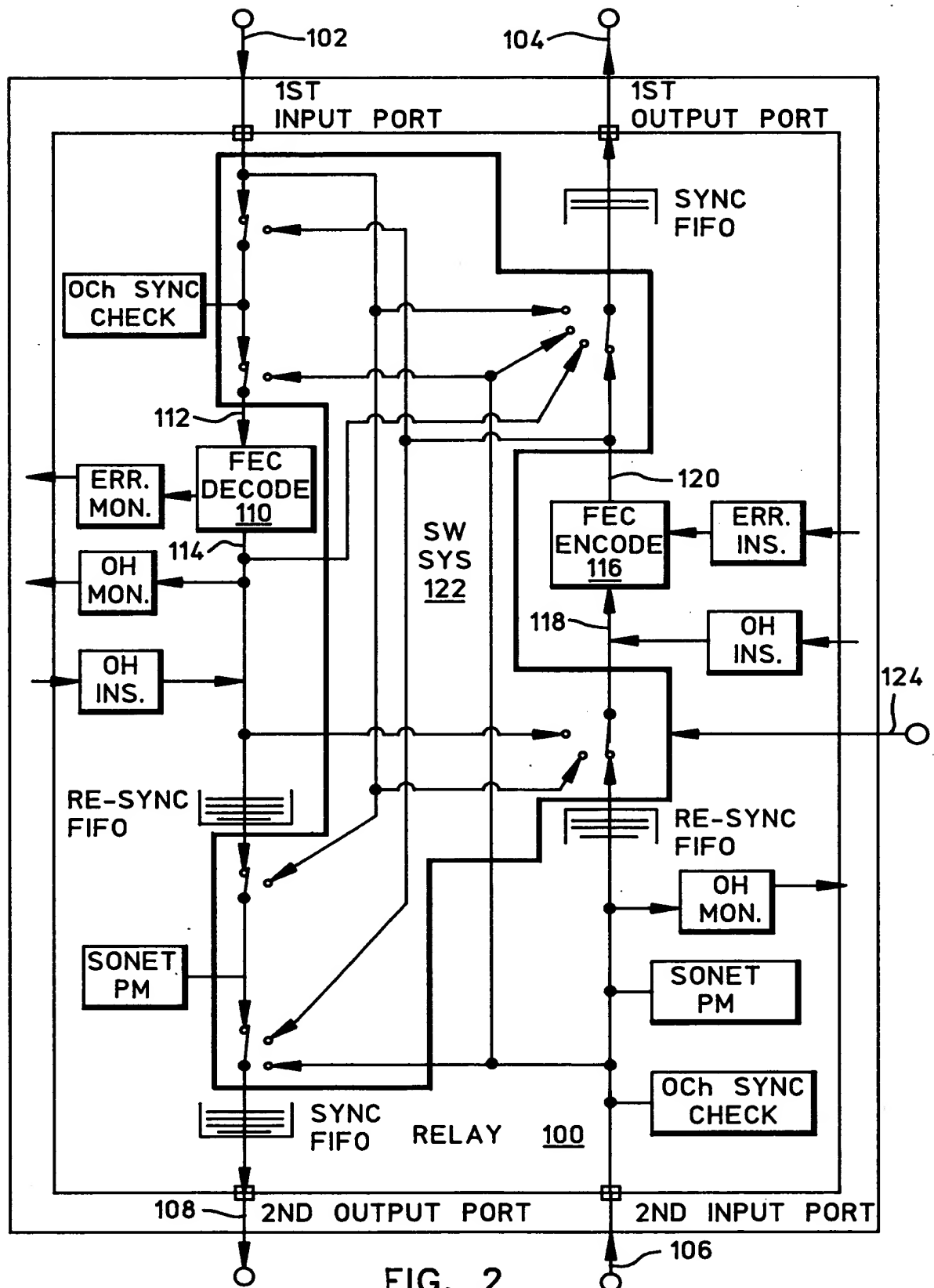


FIG. 2

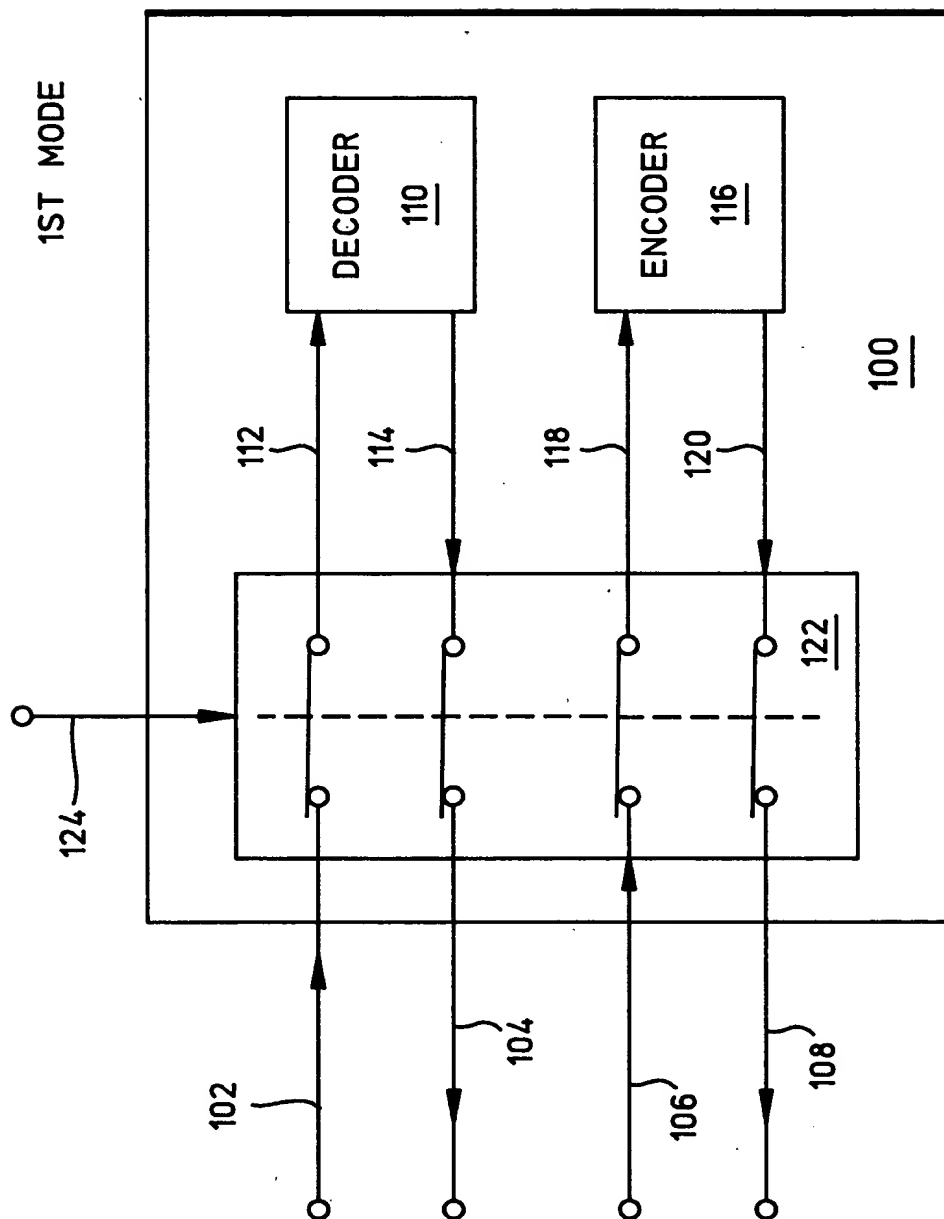


FIG. 3

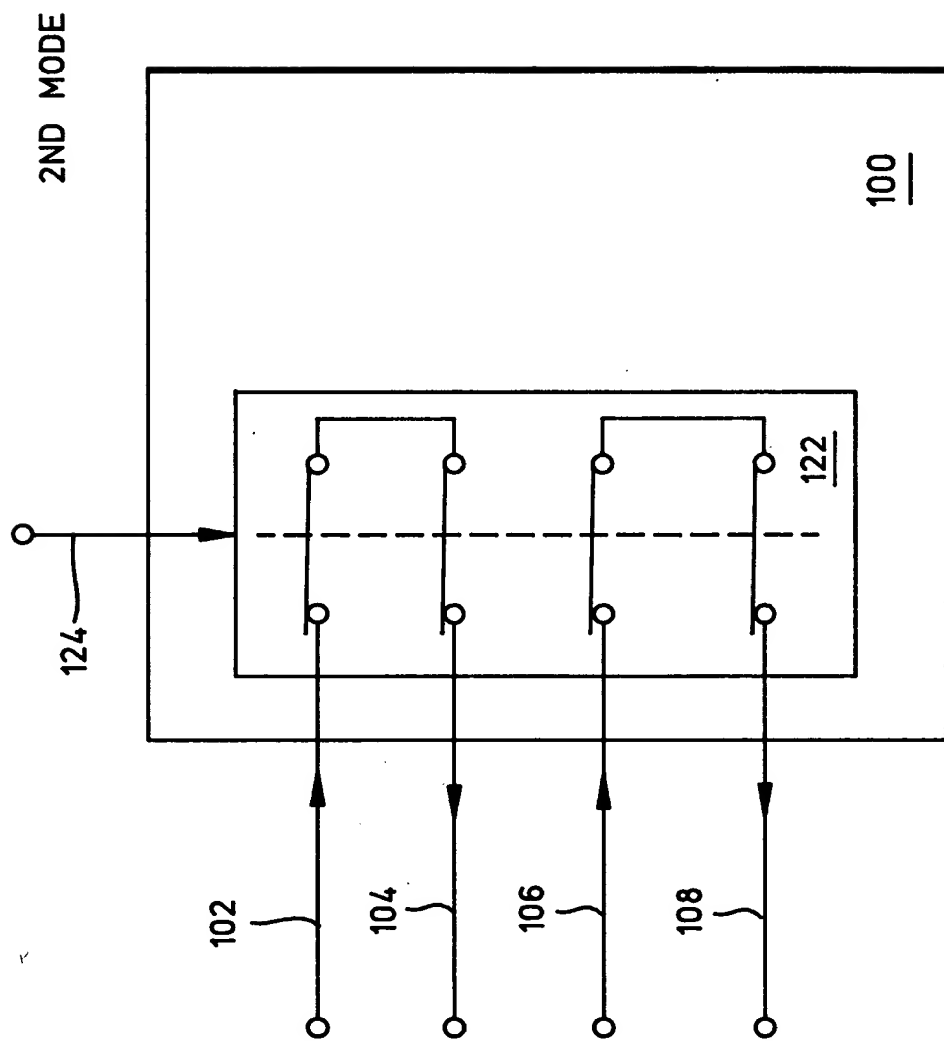


FIG. 4

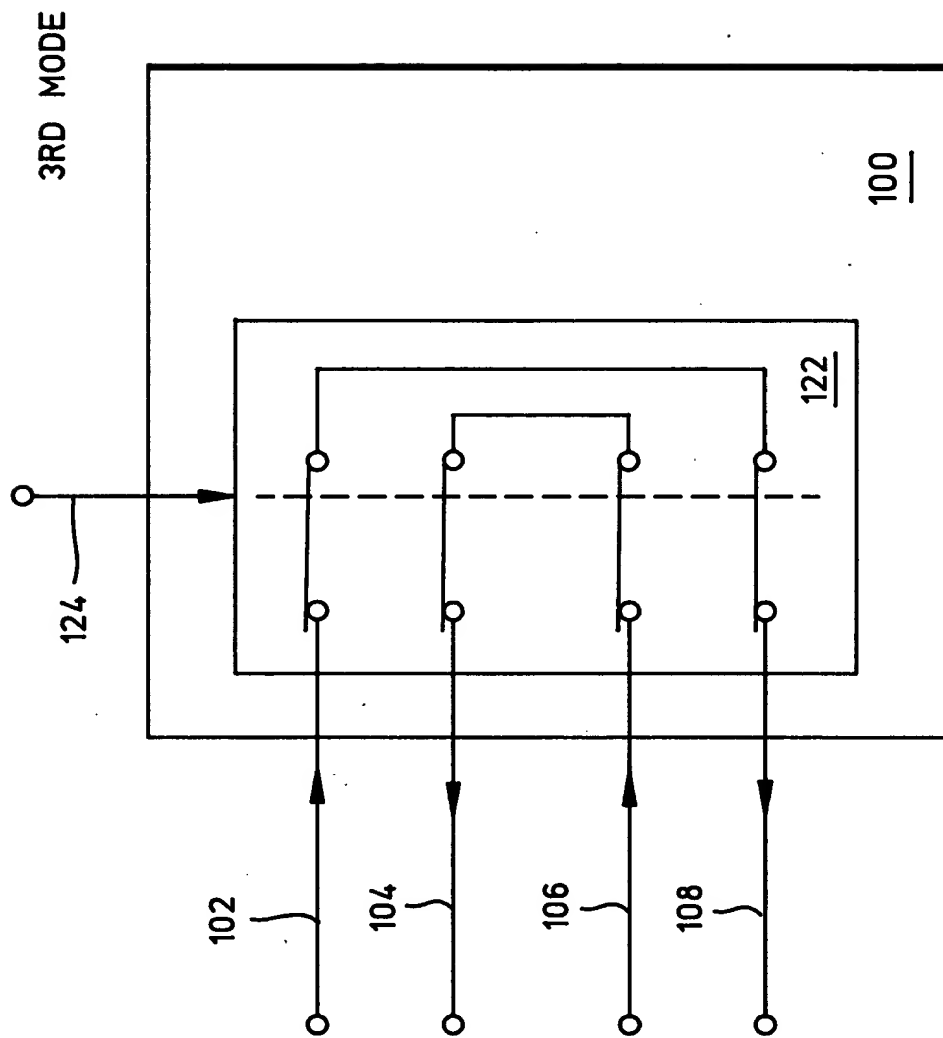


FIG. 5

FIG. 6

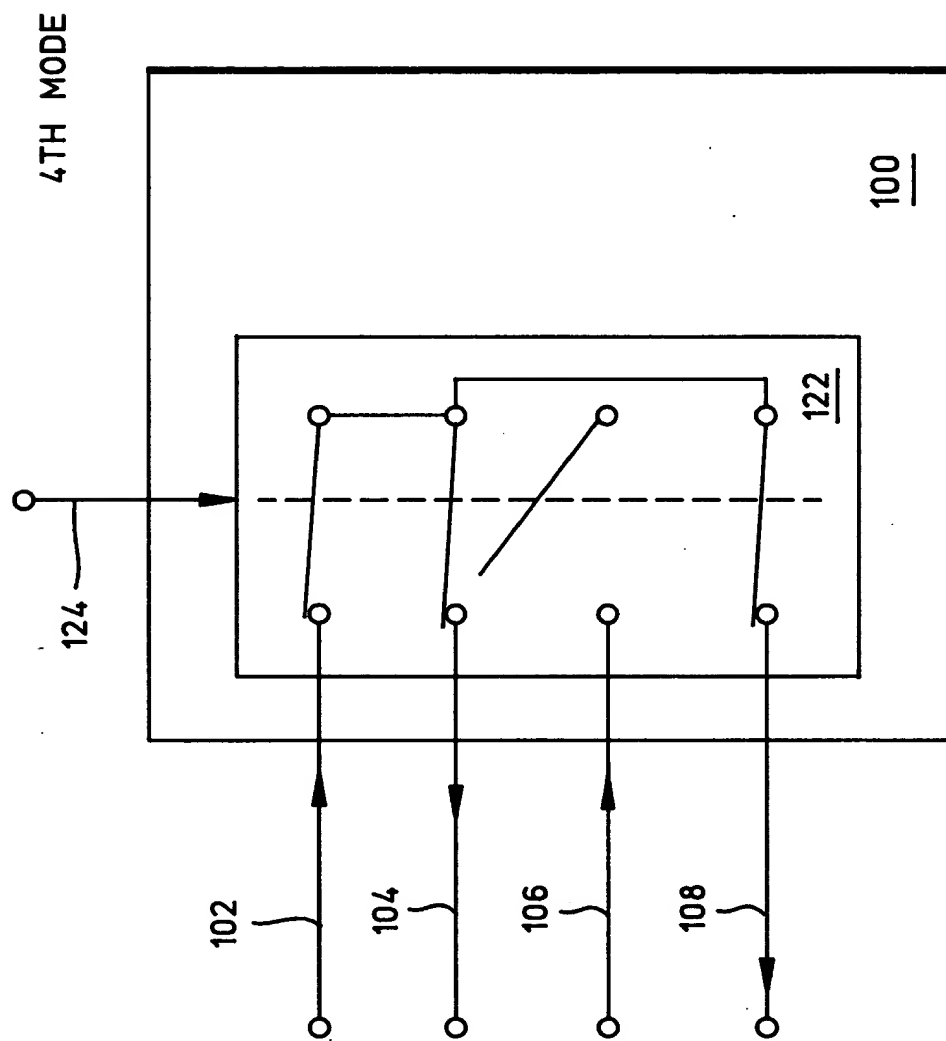


FIG. 6

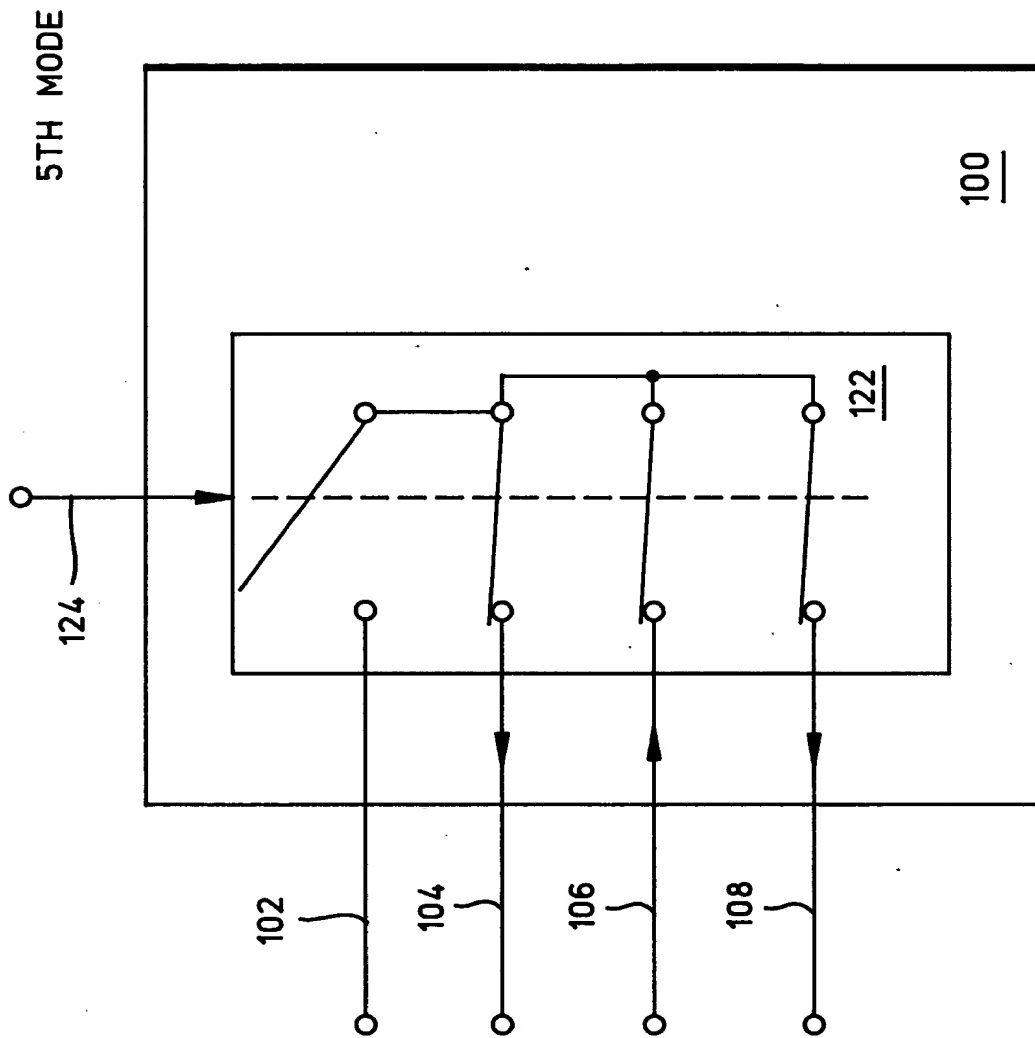


FIG. 7

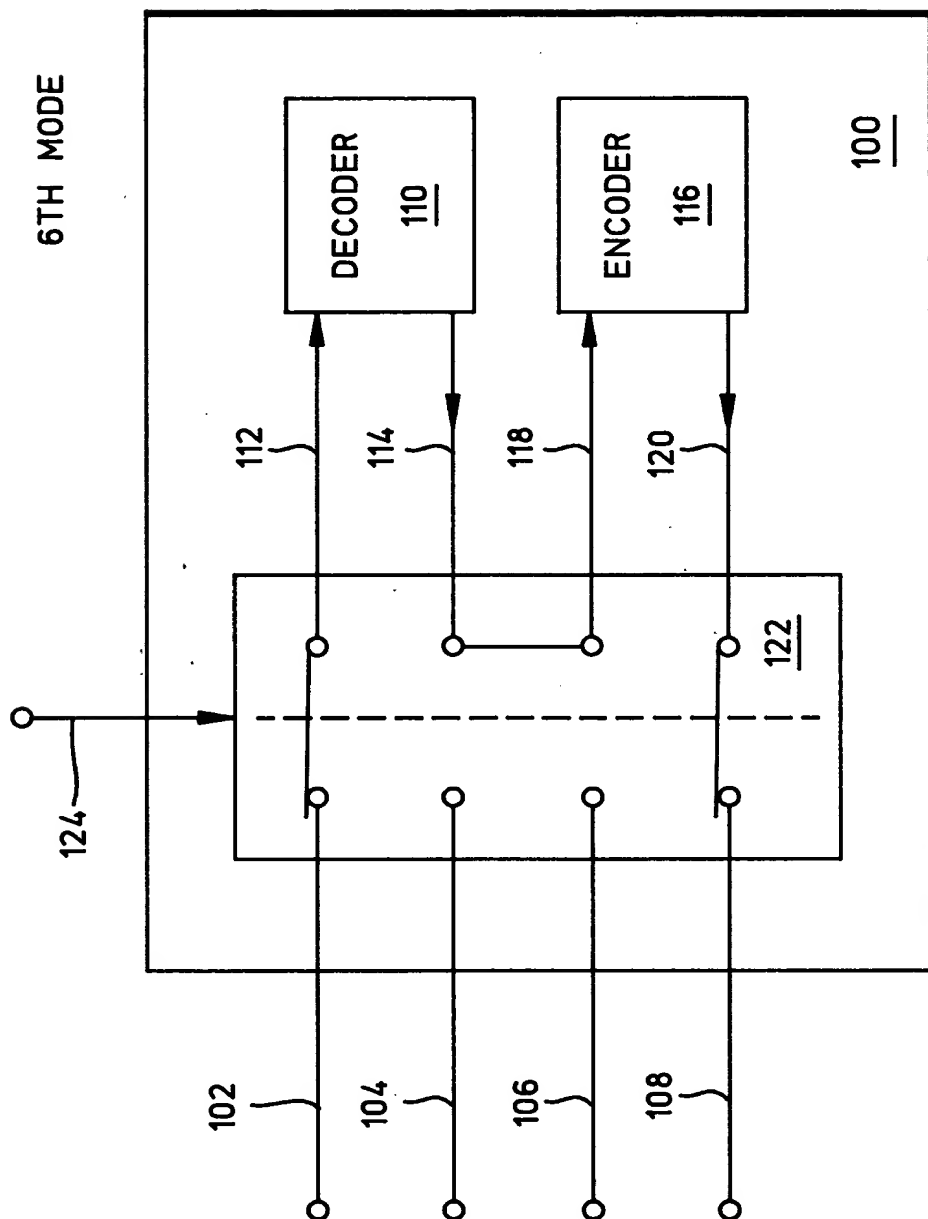


FIG. 8

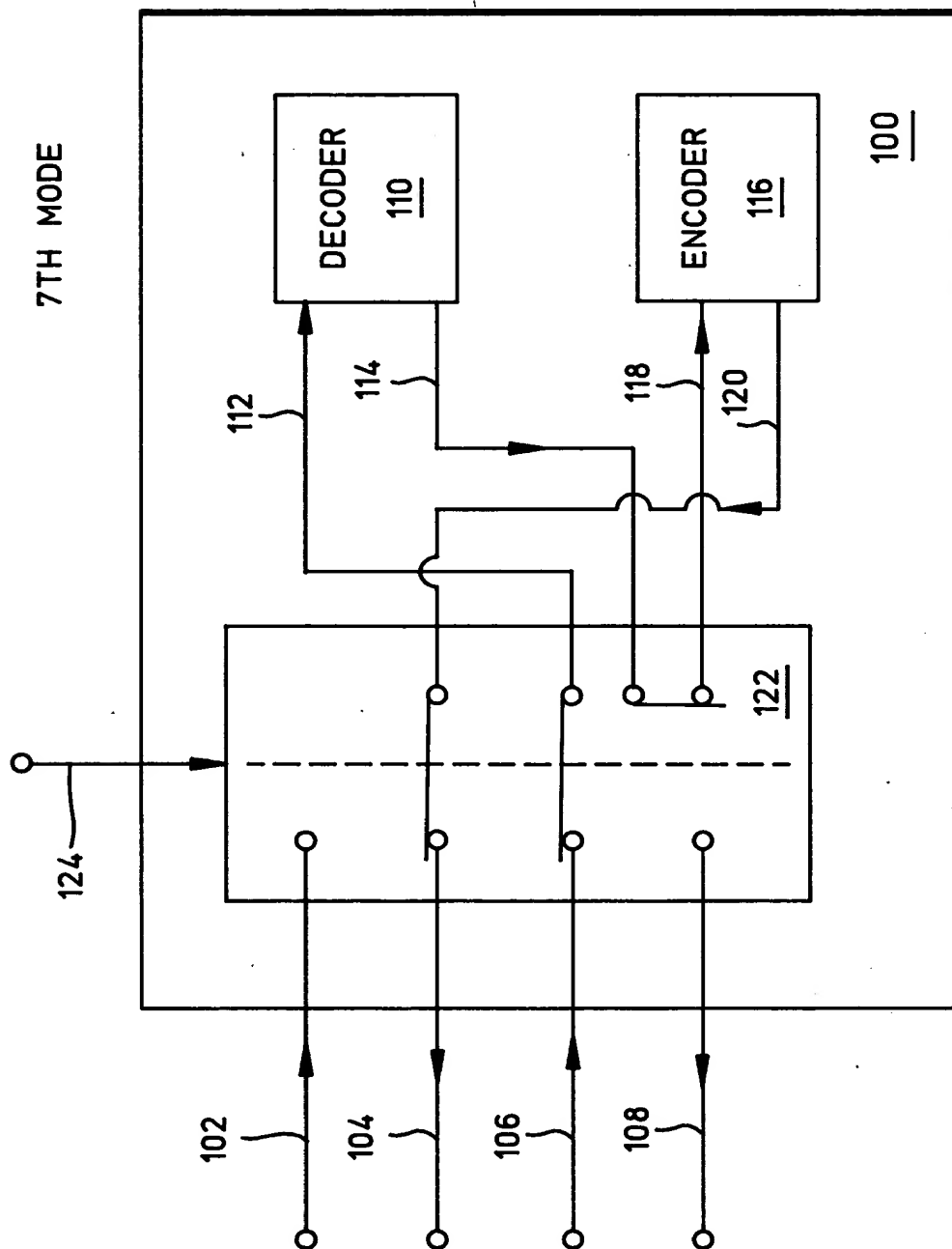


FIG. 9

FIG. 10 is a block diagram of a system 100 in 8TH MODE. The system 100 includes a DECODER 110 and an ENCODER 116. A signal 102 is input to the DECODER 110 via a switch 104. The DECODER 110 outputs a signal 112 to a switch 114. The switch 114 is controlled by a signal 124. The switch 114 outputs a signal 118 to the ENCODER 116. The ENCODER 116 outputs a signal 120 to a switch 122. The switch 122 is controlled by a signal 104. The switch 122 outputs a signal 102 to the DECODER 110. The system 100 is labeled 100.

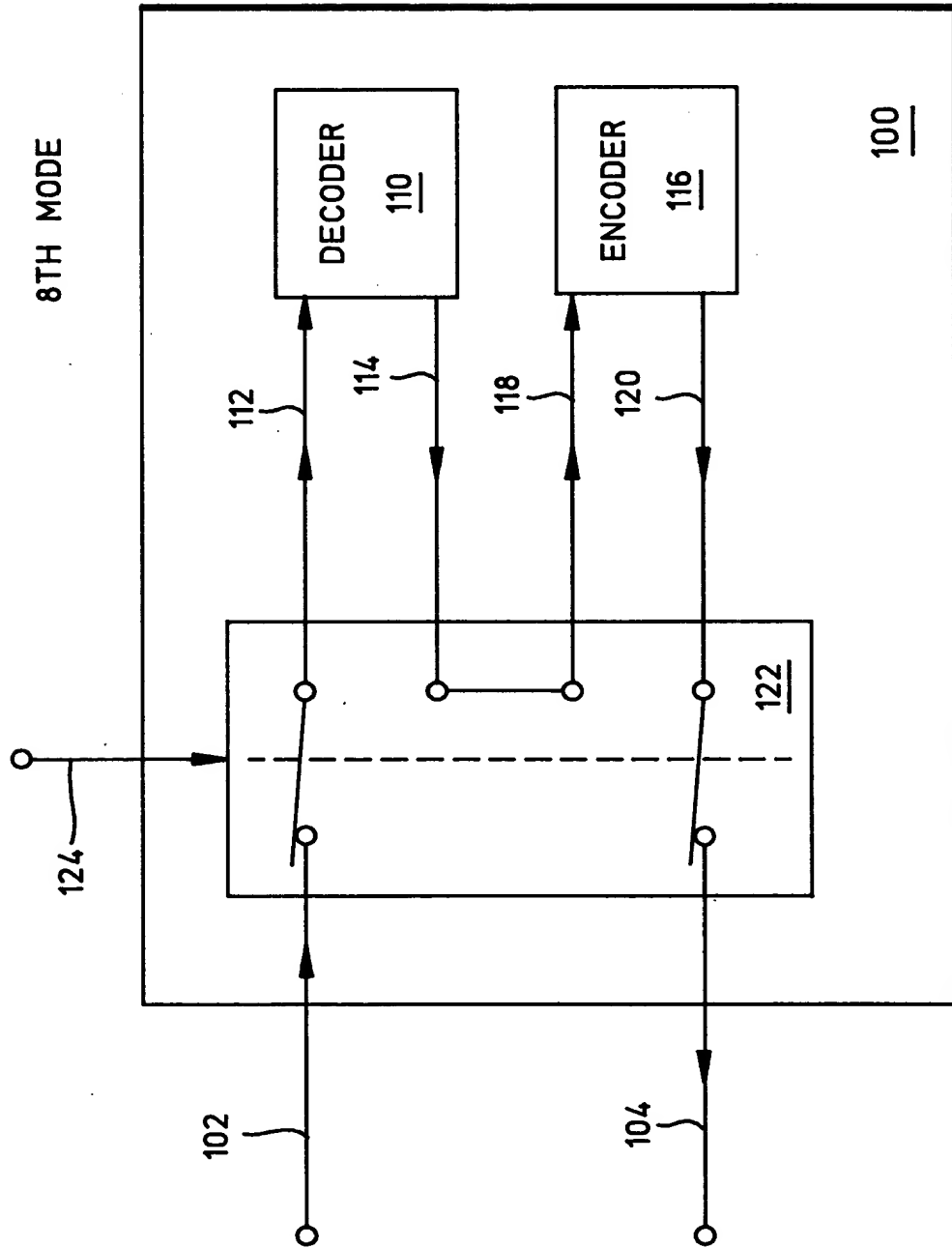


FIG. 10

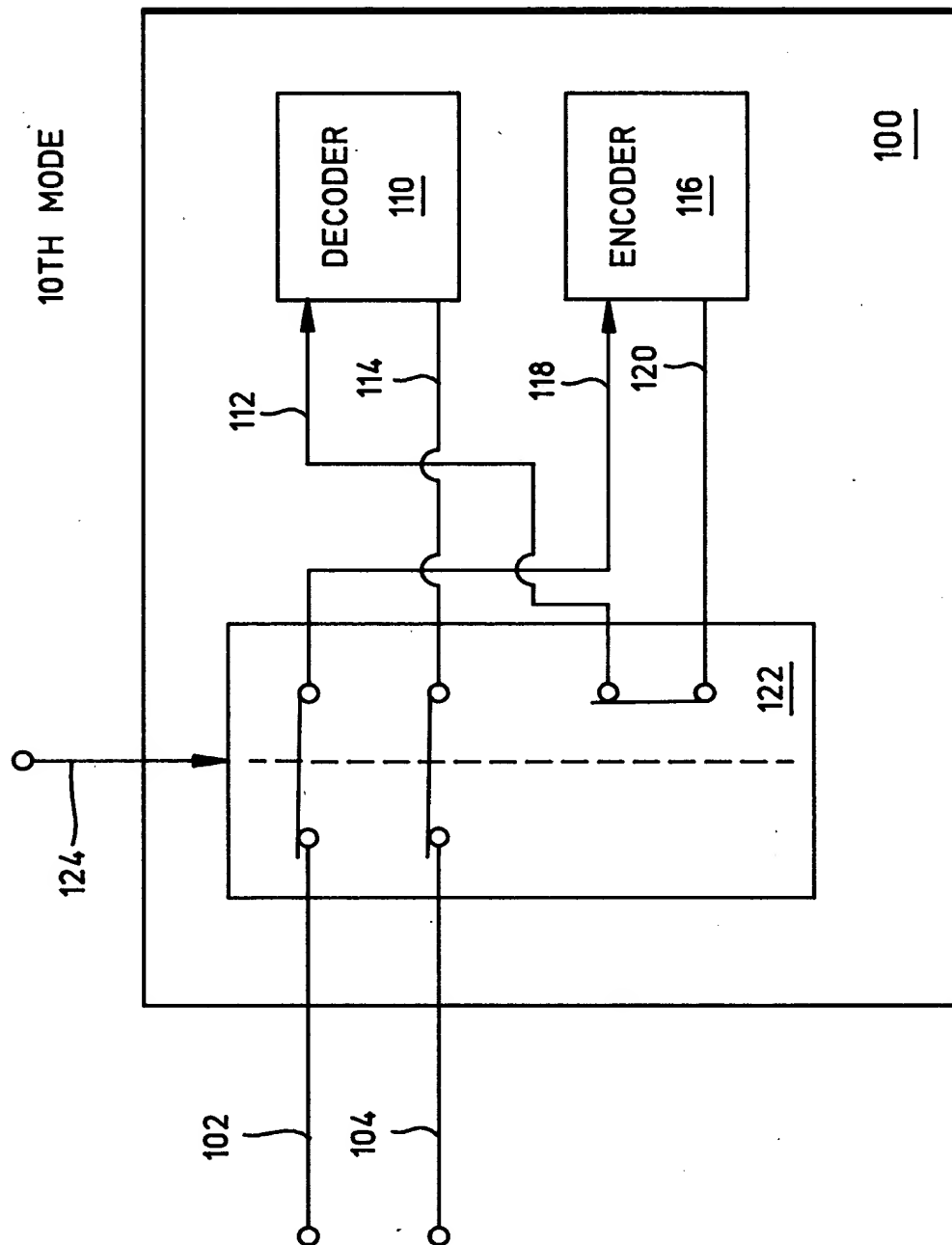


FIG. 11

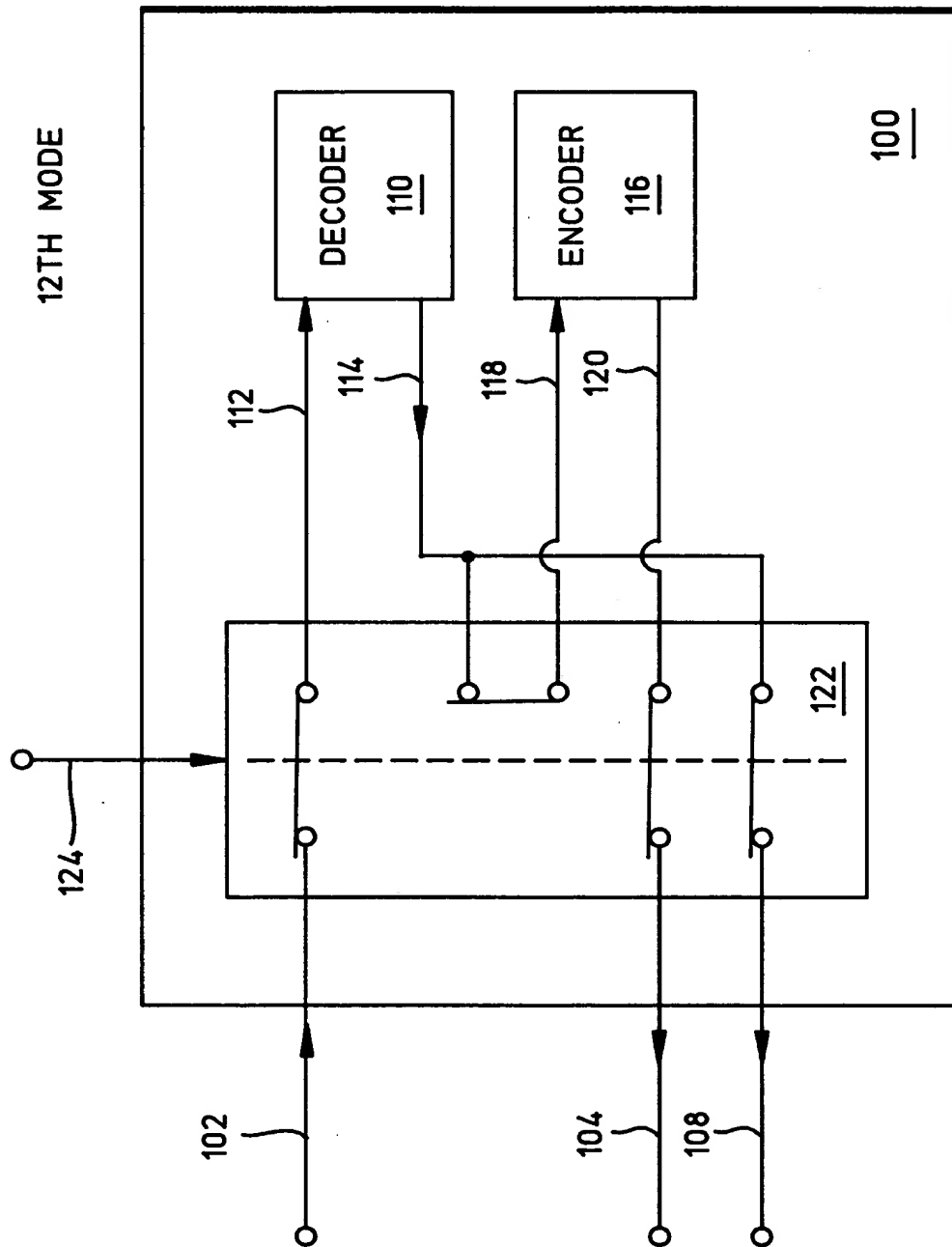


FIG. 12

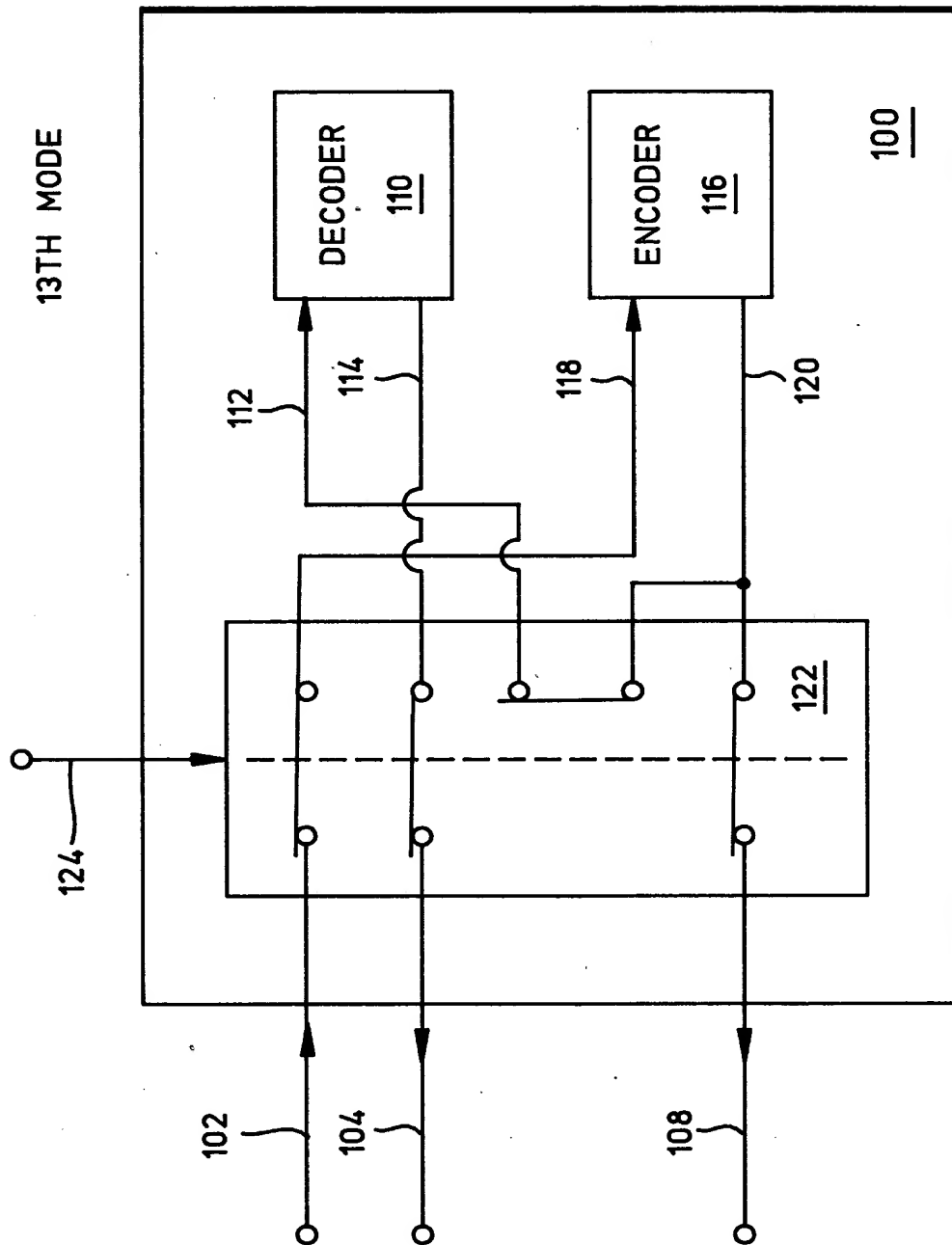


FIG. 13

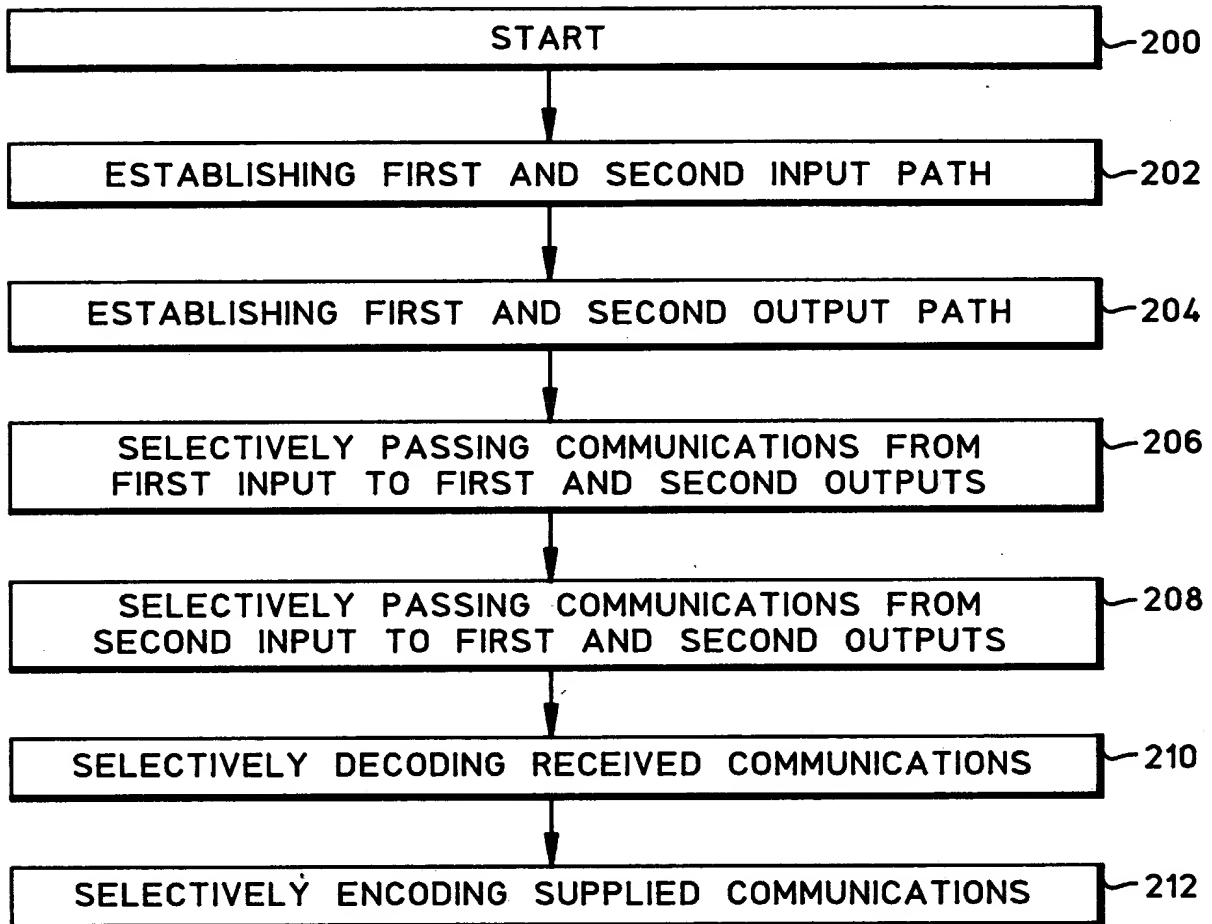


FIG. 14

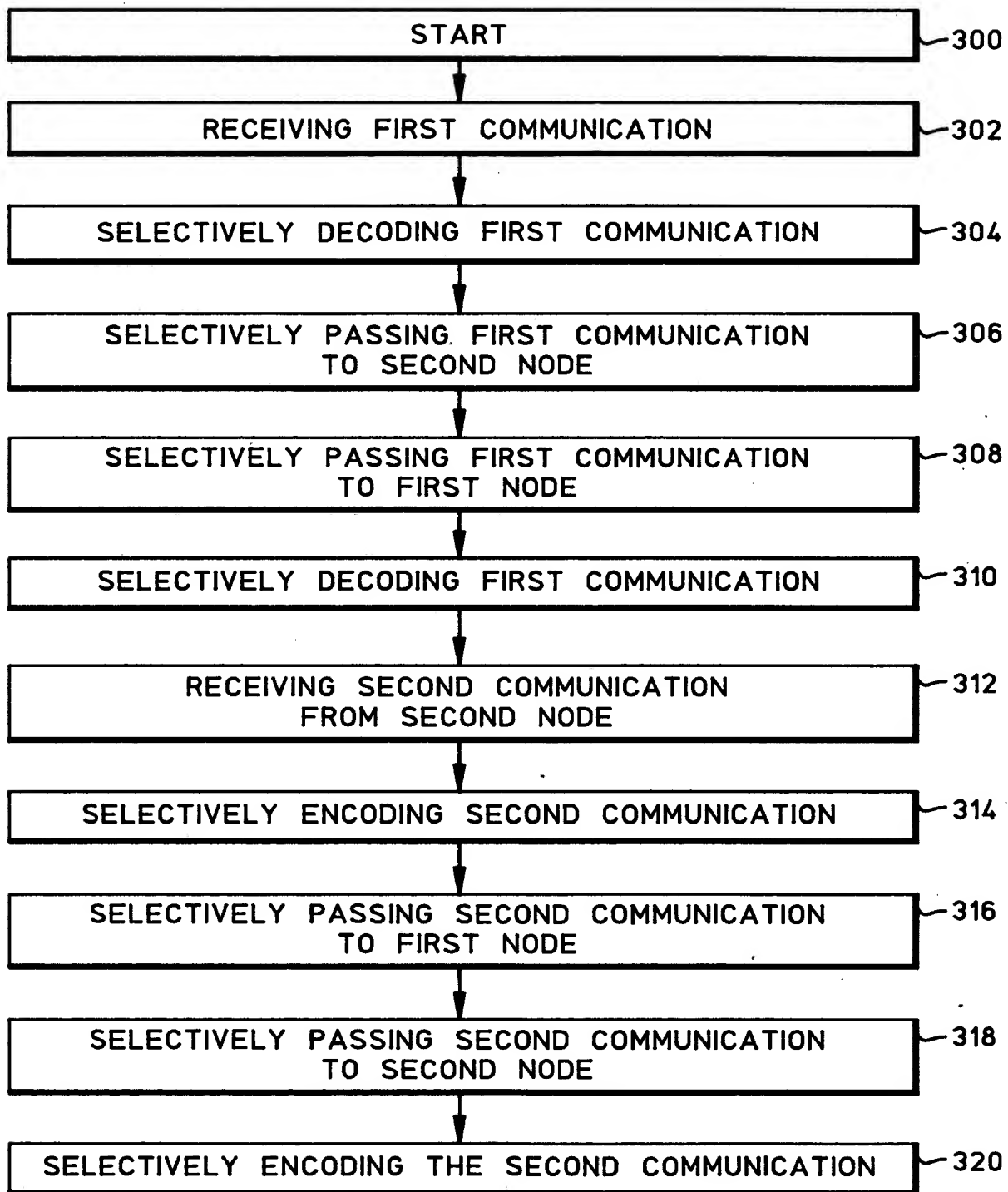


FIG. 15